

	L #	Hit	S arch T xt	DB
1	L1	3999	(361/91.1,767,768,769,770,771,777,778,779,782,783,784,785,790,791,803).ccls.	USP AT; US-P GPU B
2	L2	4520	(257/664,691,698,700,723,724,728,786).ccls.	USP AT; US-P GPU B
3	L3	1525	(333/33,247).ccls.	USP AT; US-P GPU B
4	L4	1806	324/765.ccls.	USP AT; US-P GPU B
5	L5	370	(363/144,146,147).ccls.	USP AT; US-P GPU B
6	L6	1156 2	1 2 3 4 5	USP AT; US-P GPU B
7	L7	1430	6 and @pd>=20020615	USP AT; US-P GPU B

	L #	Hit	S ar h Text	DBs
8	L8	571	7 and pin\$1	USP AT; US-P GPU B
9	L9	78	8 and (interposer\$1 adapter\$1)	USP AT; US-P GPU B
10	L10	493	8 not 9	USP AT; US-P GPU B
11	L11	859	7 not 8	USP AT; US-P GPU B
12	L12	439	11 and power	USP AT; US-P GPU B
13	L13	420	11 not 12	USP AT; US-P GPU B